TUTORIAL

Novel Transistors –
Beyond the Planar Silicon MOSFET

Organizer:
Max Lemme
University of Siegen, Germany

Conference Venue:
Messe Congress Graz, Austria
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Conference Organization:
JOANNEUM RESEARCH Forschungsgesellschaft mbH
Graz, Austria

Technical Co-Sponsorship
Novel Transistors – Beyond the Planar Silicon MOSFET

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The aim of this tutorial is to present – in a didactic format – novel and emerging transistor options for More Moore and More Than Moore applications. Even though industry is approaching the end of physical gate length scaling, the quest for new transistor designs and materials is far from over. In fact, the options for future transistors appear to be as wide as or wider than they have ever been. The speakers of this tutorial have been carefully chosen to reflect the multitude of approaches pursued in research and development today. The target audience is PhD students with various backgrounds and industry engineers, but also aims to peak the interest researchers working in related fields. The presentations will provide a thorough introduction to the respective topics and aim to give an outlook on circuit design implications. The latter is intended to also address attendants of the sister conference, the European Solid-State Circuits Conference (ESSCIRC).

Agenda:

13:00 Thin Channel Silicon Transistors
Geert Eneman, IMEC, Leuven (Belgium)

14:00 Coffee Break

14:30 Tunnel FETs
Joachim Knoch, RWTH-Aachen, Aachen (Germany)

15:30 Compound Semiconductor Devices
Suman Datta, Penn State, State College (USA)

16:30 Coffee Break

17:00 2D Channel Devices
Jörg Appenzeller, Purdue, West Lafayette (USA)

18:00 Graphene FET Models for Circuit Design
Sebastien Fregonese, University of Bordeaux, Bordeaux (France)
ESSDERC 2015 Tutorial:
Thin Channel Silicon Transistors

Geert Eneman
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Outline

- Intro: Scaling and Thin Channel MOSFETs
- Silicon-on-Insulator
- FinFETs
- Nanowires
- Conclusions
Outline

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- Silicon-on-Insulator
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The power of scaling

*Scaling ➔ more and faster transistors on chip*

<table>
<thead>
<tr>
<th>Year</th>
<th>1971</th>
<th>2015</th>
<th>ratio</th>
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</thead>
<tbody>
<tr>
<td>Transistors</td>
<td>2.300</td>
<td>1.900.000.000</td>
<td>~ 800.000</td>
</tr>
<tr>
<td>Speed (Hz)</td>
<td>10.800</td>
<td>3.800.000.000</td>
<td>~ 360.000</td>
</tr>
<tr>
<td>Gate length (nm)</td>
<td>10.000</td>
<td>~20</td>
<td>~ 1/500</td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>12</td>
<td>133</td>
<td>~ 11</td>
</tr>
</tbody>
</table>

> 40 years of scaling
MOSFET transistors

MOSFET’s: the basic component of digital logic applications

**Top-view**

**Side-view**

---

**Ideal transistor**

= switch

“On-current”

\[ V_{DS} = 1 \]

**Wanted:**

- High on-current
  - Switching time \( \tau \):
  \[ \tau \sim \frac{CV_{DD}}{I_{on}} \]
- Low off-current
  - Static power consumption:
  \[ P_{Static} \sim I_{Off} \cdot V_{DD} \]

---

**Planar Si technology**

- Essentially a 2D device: different active layers are thin
  - Only upper surface layer of Si is active
  - Thin gate insulator
  - Thin gate electrodes
- Low-topography structure: limited strain on patterning (lithography)

- Process:
  - Layer depositions \( \rightarrow \) thickness control
  - Lithography \( \rightarrow \) lateral dimension control
- Billions of transistors on one substrate
MOSFET Scaling

- Scaling has been very successful until 130nm node
- Below 130nm node: “simple scaling” becomes problematic

What we want: What we get:

- Higher on-current
- Same off-current

- Loss of channel control $\rightarrow$ off-current increases
- Increase of doping $\rightarrow$ less on-current improvement

Specified vs. actual scaling of $L_G$ and $T_{Ox}$

Scaling: slowed down due to short-channel control issues, and gate leakage
Short-channel effects

Long-channel transistors: build-up of inversion layer at the gate interface

Well-behaved transistors: inversion carriers only close to gate → good gate control

Source Drain Gate
NFET in on-state
Electrons Conduction band
Holes Valence band

Band structure along cutline

Well-behaved transistors: inversion carriers only close to gate → good gate control
Short-channel effects

Short-channel effects: channel is influenced by source/ drain regions → short-circuit from source to drain

Leakage paths in the substrate lead to poor short-channel control, e.g. poor Subthreshold Swing (SS) → increased off-state current
Short-channel effects

Solution: increase substrate doping (Well / halo implants, ground-plane)

Increased substrate doping $\Rightarrow$ better short-channel control. However, increased doping $\Rightarrow$ more junction leakage and lower mobility

Insulator cuts off source-drain leakage path.
Issues: thin Si channel $\Rightarrow$ defects, series resistance, body bias control, process control
Short-channel effects
Solution: Strain-relaxed buffers: band energies are material-dependent → band offset between channel and SRB

SRB’s band offset can improve or degrade short-channel effects / scalability.
Less band offset than SOI ↔ SRBs: easier to manufacture
Short-channel effects

Solution: FinFETs: a thin ‘fin’ channel that is controlled from 3 sides by the gate

Insulator cuts off source-drain leakage path.
Issues: thin Si channel \(\rightarrow\) defects, series resistance, body bias control, process control

Solution: Gate-All-Around / Nanowire: gate around channel \(\rightarrow\) excellent electrostatic control

Issues: thin Si channel \(\rightarrow\) defects, series resistance, body bias control, process control
Physical limits in scaling Si MOSFET

The MOSFET can be thought of as consisting of two wells (source and drain) separated by a barrier (channel).

- Planar gate: limited electrostatic control of the channel

When the channel length reduces, no effective barrier is formed between the source and drain and the transistor “OFF” current increases. Devices with an improved electrostatic control over the channel are needed.

Natural channel length $\lambda$

“A device will be free of short-channel effects if the gate length is at least 4 to 6 times longer than the natural length $\lambda$.”

Short-channel effects in MOSFETs can be minimized by:
- Decreasing the gate oxide thickness $d_{ox}$
- Increasing the dielectric constant $\varepsilon_{ox}$ of the gate oxide material. I.e. decreasing the ‘effective oxide thickness’.
- Decreasing the channel thickness $d_{channel}$ → SOI, FinFETs and nanowires

The value of the natural length is given by:

$$\lambda_1 = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{ox} t_{Si}} \quad \text{in a single-gate MOSFET}$$

$$\lambda_2 = \sqrt{\frac{\varepsilon_{Si}}{2 \varepsilon_{ox}} t_{ox} t_{Si}} \quad \text{in a double-gate MOSFET}$$

$$\lambda_4 = \sqrt{\frac{\varepsilon_{Si}}{4 \varepsilon_{ox}} t_{ox} t_{Si}} \quad \text{in a gate-all-around (quadruple-gate) MOSFET}$$

$\varepsilon_{ox}$: electrical permittivity of the gate oxide

$\varepsilon_{Si}$: electrical permittivity of the channel

$t_{ox}$: gate oxide thickness

$t_{Si}$: channel thickness

The most interesting information that can be extracted from the calculation of the natural length for the different gate configurations is that:

$$\lambda_2 = \sqrt{\frac{1}{2}} \lambda_1 \quad \text{and} \quad \lambda_4 = \sqrt{\frac{1}{4}} \lambda_1$$

It has been shown, using extensive numerical simulations, that the natural length for a tri-gate device is given by:

$$\lambda_3 = \sqrt{\frac{1}{3}} \lambda_1$$

The concept of an ‘effective gate number’, $N$, can thus be defined, and the generalized relationship for the natural length can be written as follows:

$$\lambda_N = \sqrt{\frac{\varepsilon_{Si}}{N \varepsilon_{ox}} t_{ox} t_{Si}}$$
Multigate MOSFETs

Outline

- Intro: Scaling and Thin Channel MOSFETs
- Silicon-on-Insulator
  - Properties, advantages and challenges
  - Wafer fabrication
  - Strain
  - Circuit implications
- FinFETs
- Nanowires
- Conclusions
SOI devices

Conventional bulk MOSFET

SOI MOSFET

Silicon-On-Insulator (SOI): thin channel on top of SiO\textsubscript{2} on top of Si substrate

Silicon channel

Silicon substrate

Silicon dioxide

SOI MOSFET


SOI advantage #1: Improved scalability, especially for thin channels (small t\textsubscript{Si}) → Allows shorter transistors, and low-voltage operation

Drain-Induced Barrier Lowering

O. Weber et al, Leti / ST, ECS Trans. 22(1), 78, 2009
SOI devices

Conventional bulk MOSFET

SOI MOSFET

SOI advantage #2-#3:
- Lower junction leakage \( \rightarrow \) reduced static power
- Lower junction capacitance \( \rightarrow \) increased speed

Silicon substrate

Silicon dioxide

Si: \( \varepsilon = 11.7 \)

SiO\(_2\): \( \varepsilon = 3.9 \)

Classification of SOI devices

Conventional MOSFET

Partially depleted SOI MOSFET

Partially-depleted SOI:
- Silicon film thickness greater than bulk depletion width (i.e. >40-80nm)
- Risk for kink effects
- Similar device operation as conventional MOSFETs
Classification of SOI devices

Conventional MOSFET
- Silicon substrate

Partially depleted SOI MOSFET
- Floating body
- Silicon dioxide
- Silicon substrate

Fully depleted SOI MOSFET
- Silicon dioxide
- Silicon substrate

Fully-depleted SOI:
- Silicon film thickness lower than bulk depletion width
- Channel parameters depend on substrate bias

SOI devices

Bulk transistors
“Latch-up is the inadvertent creation of a low-impedance path between the power supply rails of a MOSFET circuit, triggering a parasitic structure which disrupts proper functioning of the part”

SOI transistors
UTBSOI advantage #4-#5:
- No parasitic bipolar/thyristor → no latch-up
- Isolation from substrate → good radiation hardness

Fully-depleted SOI:
- Silicon film thickness lower than bulk depletion width
- Channel parameters depend on substrate bias
  → SOI advantage #6: back bias can be used for $V_T$ tuning.
  High-performance, low-leakage, ... device flavors

SOI: Channel Doping and Variability

- Thick channels: $V_T$ can be tuned by channel doping.
  Similar to bulk FETs.
- Thin channels: $V_T$ independent of doping
  → No channel doping required in UTBSOI

SOI: Channel Doping and Variability

Threshold voltage ($V_T$) vs channel thickness

Random dopant fluctuations are an important source of variability
→ SOI advantage #7: low channel doping → low $V_T$ variability, high mobility

SOI: Access Resistance

Thin source/drain portions under the channel are a concern for access resistance

Careful junction design, thin spacers and epitaxial source/drains are a must for UTBSOI. Series resistance reduction is more critical than for bulk technologies
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SOI devices: Substrate Fabrication

SOI substrate techniques

- SIMOX (Separation by IM implanted OXygen)
- Smart-Cut®
- BESOI (Bond and Etch-back SOI)
- ELTRAN® (Epitaxial Layer TRANsfer)
- SOS (Silicon-On-Sapphire)
- ...

SOI devices: Substrate Fabrication

SOI substrate techniques

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- SOS (Silicon-On-Sapphire)
- ...


SOI Formation: SIMOX Process

1. Initial silicon

2. Oxygen implant

- Energy 120-200 keV
- Dose ~0.3-1.8e18 cm⁻²

3. Anneal

- >1300°C, 3-6 hours
SOI Formation: SMART-CUT® Process (Soitec, CEA-Leti)

1. Initial silicon

2. Oxidation

3. Smart-Cut implant

   \[ \text{H}^+ \text{ ions } 5 \times 10^{16} \text{ cm}^{-2} \]

4. Cleaning and bonding

   \[ \text{Wet clean or plasma treated bonding} \]

5. SmartCut splitting at 500°C

6. Annealing 1100°C + CMP

7. Wafer A becomes B

SOI: What about Strained Channels?

Mechanical strain is a performance booster for planar FETs since the 90nm node

- Global strain: e.g. virtual buffers
SOI: What about Strained Channels?

Mechanical strain is a performance booster for planar FETs since the 90nm node

- Global strain: e.g. virtual buffers

**Planar technology**

- Strained Si channel
- SiGe virtual substrate
- Source
- Drain

**SOI technology**

- Strained Si channel
- SiO₂ Silicon
- Source
- Drain

**Strained SOI wafers (SOITEC)**

1. Initial silicon
2. Oxide formation
3. Smart-Cut implant
4. Cleaning and bonding
5. SmartCut splitting at 500°C
6. SiGe Selective etch
7. Finished sSOI wafer

Global stress techniques compatible with SOI technology

- CESL compatible with SOI technology

A. Thean, VLSI Symp., 2006
SOI: What about Strained Channels?

Mechanical strain is a performance booster for planar FETs since the 90nm node

- Local strain: Contact etch-stop layers (CESL), source/drain (S/D) stressors
- CESL compatible with SOI technology
- SiGe S/D stressor: no S/D etch possible \(\rightarrow\) not optimal

Strained CESL

\[
\text{Si}_{1-x} \text{Ge}_x
\]

Planar technology

SOI technology

\[
\text{SiO}_2
\]

SOI: More Design Considerations

- Lower S/D cap, lower parasitics to ground \(\rightarrow\) Improved frequency response
- Reduced latch-up, improved substrate immunity
- Improved high-T operation (due to lower leakage)
  - Passive components can be different:
    - SOI well resistor has no parasitic diode, lower capacitance to ground
    - No well capacitance in SOI
    - Inductors have higher Q factor (high-resistive substrate)
- No conventional diodes available. Gated diodes are an alternative.
- Floating body effects (PDSOI)
- Poor thermal response (buried oxide). Self heating.

Bulk

Well contact

\[\text{P-type Substrate}\]

n - well

Well contact

SOI

Contact

\[\text{Oxide}\]

\[\text{Substrate}\]

A. Thean, VLSI Symp., 2006

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- Silicon-on-Insulator
  - FinFETs
    - Properties and advantages
    - Access resistance and junctions
    - Effective width and mobility
    - Strain
    - Circuit implications
- Nanowires
- Conclusions

SOI and FinFETs

SOI and FinFETs both get their excellent scalability from an ultra-thin channel

FinFETs / Tri-Gate FETs

FinFETs can be fabricated on SOI or bulk substrates

SOI-FinFET

Bulk-FinFET

Shallow-trench isolation

Bulk-FinFETs can use standard wafers (cost)
FinFETs / Tri-Gate FETs

FinFETs can be fabricated on SOI or bulk substrates

Bulk-FinFETs can use standard wafers (cost), but require isolation of the substrate (well doping, barrier layer, ...)

Subthreshold slope vs gate length

**Excellent scalability**
FinFETs / Tri-Gate FETs

FinFETs have similar advantages as SOI FETs

- Excellent scalability
- High-resistive path to substrate
- Low junction leakage
- Low junction capacitance
- Robust against latch-up and radiation


Inverter delay vs fin height

Inverter delay vs fin height


- Excellent scalability
- High-resistive path to substrate
- Low junction leakage
- Low junction capacitance
- Robust against latch-up and radiation
  - Back bias for $V_T$ tuning?
FinFETs / Tri-Gate FETs

FinFETs have similar advantages as SOI FETs

Threshold voltage vs fin width

- Excellent scalability
- High-resistive path to substrate
- Low junction leakage
- Low junction capacitance
- Robust against latch-up and radiation
- Back bias for $V_T$ tuning?
- Lowly-doped channels \(\rightarrow\) reduced random-dopant fluctuation, good mobility

N. Collaert et al., VLSI Symp. 2005

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FinFETs: Access resistance

Current travels from source \(\rightarrow\) drain. In the extension it passes through a fin which is lightly-doped and not gate-controlled \(\rightarrow\) High extension resistance

![SOI FinFET Diagram](image)

Extension region: under the spacer

FinFETs: Junctions

Implanted dopants may lead to non-uniform source/drains (S/D)

Top-Only S/D  
Conformal S/D

<table>
<thead>
<tr>
<th>Drive current</th>
<th>$I_{DS} - V_{GS}$ Comparison</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}=1.2V$</td>
<td></td>
</tr>
</tbody>
</table>

Conformal extensions result in up to 2 x $I_{drive}$ increase!

Junction design is critical for fins. 
Source/drains need to be conformally doped
FinFETs: Junctions

Strong dependence of performance on implant angle
→ High angles required for uniform fin doping... but high angle implants cannot be used in high density circuits

FinFETs: Junctions

‘Shadowing’ of implants due to neighboring fins and resist

In dense layouts (e.g. SRAM), high-angle implants are shadowed by neighboring fins or resist
**FinFET Access Resistance: Extensions**

E.g. plasma doping as alternative:

- Blanket epitaxial raised S/D growth
- Selective undercut Etch pMOS regions
- In-situ doped p⁺ SiGe epitaxy

Dual epi raised S/D for non-planar tri-gate

- Compressive Strain and Rs/D Reduction

Epi-grown S/D requires to reduce access resistance

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*J. Kavalieros et al, Intel, VLSI 2006*
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FinFETs and Effective Width

FinFETs: Conduction through top and side of channel

\[ I \approx C_{Ox} \frac{W_{Eff}}{L} \cdot \mu \cdot (V_{GS} - V_T)^\alpha \]

Can offer higher drive current than planar
(depending on distance between fins, fin height, etc...)
FinFETs and Effective Width

A channel is formed at the top and sidewalls of the fin

Electrical vs. physical FET width (Fin-Effect)

\[ I \approx C_{ox} \frac{W_{eff}}{L} \cdot \mu \cdot (V_{GS} - V_{T})^\alpha \]

Carrier mobility

FinFETs and Effective Width

Fin top and side are different crystallographic planes and have different carrier mobilities
- Fin top: (100)/<110> plane
- Fin side: (110)/<110> plane

Top channel (100)/<110>
Side channel (110)/<110>

Top channel

Side channel
**FinFETs: Orientation-Dependent Mobility**

Experimental work, SiON dielectric, long channels

<table>
<thead>
<tr>
<th>Silicon</th>
<th>Electrons</th>
<th>Holes</th>
</tr>
</thead>
<tbody>
<tr>
<td>(100)&lt;110&gt;</td>
<td>237</td>
<td>58</td>
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<tr>
<td>(110)&lt;110&gt;</td>
<td>88</td>
<td>168</td>
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<tr>
<td>(110)&lt;100&gt;</td>
<td>107</td>
<td>106</td>
</tr>
<tr>
<td>(111)&lt;112&gt;</td>
<td>154</td>
<td>92</td>
</tr>
</tbody>
</table>


Fins: What about Strained Channels?

Mechanical strain is a performance booster for planar FETs since the 90nm node

For realistic fin widths (W<30nm), perpendicular channel stress is negligible

→ Virtual substrates are uniaxial stressors in FinFETs

(←→ planar MOSFETs: biaxial stress)

Most stressors are compatible with (bulk) fins, with different channel stress
FinFETs: More Design Considerations

Similarities to planar SOI:

- Lower S/D cap, lower parasitics to ground \( \rightarrow \) Improved frequency response
- Reduced latch-up, improved substrate immunity
- Improved high-T operation (due to lower leakage)

- Passive components can be different:
  - SOI-FF well resistors have no parasitic diode, lower capacitance to ground
  - No well capacitance in SOI-FF
  - Inductors have higher Q factor (high-resistive substrate)

- No conventional diodes available in SOI-FF. Gated diodes are an alternative.
- Poor thermal response (SOI-FF). Self heating.

\[ \text{SOI-FinFET} \]
\[ \text{Bulk-FinFET} \]

\[ \text{Si fin} \]
\[ \text{SiO}_2 \]
\[ \text{Si sub} \]

Thin-Fin FETs: More Design Considerations

- Potentially higher drive current per area than planar
- Fin pitch \( (P_{\text{fin}}) \) and fin height are fixed by process
  \( \rightarrow \) Discrete number of fins \( \rightarrow \) quantized ‘device width’
- Gate-to-S/D parallel plate transistor \( \rightarrow \) higher gate-to-source/drain (Miller) capacitance
- Using back-bias for multi-\( V_T \) is difficult

\[ \text{Bulk-Si MOSFET} \]
\[ \text{FinFET} \]

\[ \text{D} \quad \text{G} \quad \text{S} \]
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- Intro: Scaling and Thin Channel MOSFETs
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  - Properties, advantages and disadvantages
  - Fabrication
  - Design considerations
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Evolution of transistors towards devices with improved electrostatic control
Comparison of Planar vs Nanowire Architecture

Planar MOSFET

- Planar gate:
  limited electrostatic control of the channel

  \[ \lambda = \sqrt{\frac{\varepsilon_{\text{ch}}}{\varepsilon_{\text{ox}}} d_{\text{ox}} d_{\text{channel}}} \]

- Example:
  8 nm SOI, 1 nm SiO2: \( \lambda \approx 5 \text{ nm} \)
  \( \Rightarrow L_0 > 20 \text{ nm} \)

⇒ NW device geometry yields improved scaling and better inv. subthreshold slope

Heike Riel, IBM, Sinano Workshop, Seville (2010)

Nanowire MOSFET:

- Surround gate (Nanowire):
  ultimate electrostatic control of channel

  \[ \lambda = \sqrt{\frac{\varepsilon_{\text{nw}} d_{\text{nw}}^2}{8 \varepsilon_{\text{ox}}} \ln \left(1 + \frac{2d_{\text{ox}}}{d_{\text{nw}}}\right)} \]

- Example:
  8 nm SiNW 1 nm SiO2: \( \lambda = 2.3 \text{ nm} \)
  \( \Rightarrow L_0 > 9 \text{ nm} \)

Heike Riel, IBM, Sinano Workshop, Seville (2010)
Nanowires

Nanowire advantages

Subthreshold slope vs gate length

- Excellent scalability, better than fins or planar SOI
- High-resistive path to substrate →
  - Low junction leakage
  - Low junction capacitance
  - Robust against latch-up and radiation
- Back bias for $V_T$ tuning?
- Lowly-doped channels → reduced random-dopant fluctuation, good mobility

C. Hobbs, Sematech Symposium, 2011

Nanowires: Disadvantages

- Series resistance: more challenging than fins or SOI
- Current scales down with wire cross-section → stacked wires required to have enough drive
- Processing: controlled etching of wires required. Top-to-bottom wire variation?
- Can the channels be stressed?
- New sources of variability

Variability in Si nanowires

J. Zhuge, IEDM, p.61, 2009
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Nanowire Fabrication

Wong – NUS Singapore – VLSI 2009

Bangsaruntip – IBM – IEDM 2009
Nanowire Fabrication

Stacking nanowires helps increase total drive current to meet ITRS targets.

C. Hobbs, Sematech Symposium, 2011

Nanowire Fabrication

Yeo – Samsung – IEDM 2006

Dupre – CEA-LETI – IEDM 2008
Wires: More Design Considerations

**Similarities to FinFETs:**
- 🙄 Lower S/D cap, lower parasitics to ground → Improved frequency response
- 🙄 Reduced latch-up, improved substrate immunity
- 🙄 Improved high-T operation (due to lower leakage)
  - Passive components can be different:
    - SOI-wires well resistors have no parasitic diode, lower capacitance to ground
    - No well capacitance in SOI-wires
    - Inductors have higher Q factor (high-resistive substrate)
- ☹️ No conventional diodes available in SOI-wires. Gated diodes are an alternative.
- ☹️ Poorer thermal response than fins. Self heating.

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**Wire pitch ($P_{fin}$) and # of stacked wires are fixed by process**
- Discrete number of wires → quantized ‘device width’

**Gate-to-S/D parallel plate transistor worse than fins**
- higher gate-to-source/drain (Miller) capacitance

**Using back-bias for multi-$V_T$ is difficult**

---

**Potential drive current per area than planar**

- Wire pitch ($P_{fin}$) and # of stacked wires are fixed by process
  - Discrete number of wires → quantized ‘device width’
  - Gate-to-S/D parallel plate transistor worse than fins → higher gate-to-source/drain (Miller) capacitance
  - Using back-bias for multi-$V_T$ is difficult

---

Conclusions

- An overview is given of SOI, FinFET and nanowire technologies and their difference with planar FETs
- Trade-off between scalability, better substrate isolation/variability ↔ wafer cost, process complexity, access resistance, etc.
- Circuit design with SOI/fins: similar to bulk, however optimization is required between technologies
- Post-28nm nodes use UTB-SOI and FinFETs. Post-14nm nodes: nanowires?
- Thank you for your attention!
COMPOUND SEMICONDUCTOR DEVICES

Conference Sponsors:

Computing gets cheaper and energy efficient

2 X energy efficiency increase every 1.5 years
VOLTAGE SCALING

Constant field scaling worked before
Recent years, voltage scaling has slowed down

\[ I_{on} = C_{gate} v_{eff} (V_{dd} - V_{th}) \]
\[ I_{off} = I_o 10^{-V_{th}/SS} \]

CHALLENGES

\[ E = \frac{1}{2} C_{gate} V_{DD}^2 \alpha + I_{leak} V_{DD} T \]

- increase \( v_{eff} \)
- reduce SS
SI CMOS

Drain Current, $I_{DS}$ [µA/µm]

Gate Voltage, $V_{GS}$ [V]

PMOS

NMOS

$V_{GS}$ = 0.05V

$V_{DS}$ = 0.8V

$V_{GS}$ = 0.8V

Open Symbol

Closed Symbol

$L_g$ = 26nm

EOT = 0.9nm

Intel 22nm

Simulation

C. Auth et al VLSI 2012

3D Continuum model (modified drift-diffusion and quantum corrected density gradient approximation) captures $I_d$-$V_g$

INJECTION VELOCITY IN SI CMOS

Injection Velocity, $v_{inj}$ [x10⁷ cm/s]

NMOS

PMOS

$V_{CC}$ [V]

Injection Velocity, $v_{inj}$ [x10⁷ cm/s]

NMOS

PMOS

Sheet Charge, $n_s$ [x10¹² cm⁻²]

Injection velocity in the range of 4 to 6 x10⁶ cm/s

Carrier density in the range of 6 to 8 x10¹² /cm²
“0.5V FETs with High Velocity Carriers at Low Field”

Quasi Ballistic FETs

High Performance in Ballistic Regime:
1. Low $m^*$ along channel direction $\Rightarrow$ High $v_{inj} \Rightarrow$ Maximize $I_{DSAT}^{ball}$
2. High $m_{DOS}^x$ $\Rightarrow$ High $C_{GATE}^{ball}$ $\Rightarrow$ High $Q_{INV}^{ball} \Rightarrow$ Maximize $I_{DSAT}^{ball}$

\[
I_{DSAT} = WC_G u_s(0)(V_{GS} - V_T)
\]

\[
\frac{1}{u_s(0)} = \frac{1}{v_{inj}} + \frac{1}{\mu^{eff} E(0^+)}
\]

Ballistic $\uparrow \mu^{eff}$ $\Rightarrow$ $I_{DSAT}^{ball} = W C_G (V_{GS} - V_T) u_{inj}$

\[
v_{inj} = \sqrt{\frac{2kT}{m^*}}
\]
Challenge: Lattice Mismatch

Solution: Metamorphic buffer architecture with large effective bandgap

Fully relaxed metamorphic buffer layer used for epitaxial growth of In$_{0.7}$Ga$_{0.3}$As quantum well on Silicon

M. Hudait, S. Datta et al, IEDM 2007
**MOTIVATION**

- $V_{\text{inj}}$ for III-V devices higher than Si state-of-the-art
- $V_{\text{inj}}$ for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ FinFET device lower than HEMT
- Multigate architecture required to maintain electrostatics


**But.......HEMTs are not scalable**

Double gate is the only scalable option
Multi-Gate III-V FET

III-V FinFET combining superior transport with acceptable short channel effects

MULTI-GATE III-V FET

Planar to multi-gate:
1. Side wall interface states ($D_{IT}$): SS and Coulombic scattering
2. Etch induced side wall roughness: scattering
3. Quantum confinement: $m^*$ change

A V Thathachary et al, Nano Lett. 2014
SIDEWALL ROUGHNESS

- Side wall scattering dominates transport at lower fin width

Gated Hall measurements show $\mu$ reduces with fin width for multi-gate III-V devices
- Rate of mobility roll-off depends on composition and channel architecture

III-V FF MOBILITY

A V Thathachary et al, Nano Lett. 2014
Three channel architectures chosen to study effect of In % change and confinement

 Majority inversion charge forms near the surface for In$_{0.53}$Ga$_{0.47}$As Bulk FinFET at higher overdrive

 Volume inversion expected to significantly improve QW channel performance
**Process Flow**

1. **n+ cap recess** (wet etch)
2. **Fin patterning**
3. **S/D contact**
4. **ALD High-k**
5. **1nm Al₂O₃/2.5nm HfO₂**
6. **Channel Drain**
7. **Source**
8. **S/D contact**
9. **Gate metal lift-off**

**Reducing Dᵢₜ: In-Situ Plasma Nitride Passivation**

- 3 min clean in 10:1 Buffered HF + DI rinse
- In-situ plasma pre-clean and passivation @ 250°C
- N₂ plasma/TMA pulsing: 5 cycles + 10 cycles H₂O pulsing
- 1nm Al₂O₃ + 2.5nm HfO₂ grown @ 250°C using Thermal ALD process
- 70nm thermal Nickel evaporation for gate metal
- 350°C FGA for 20 mins

- Plasma AlOₓNᵧ passivation layer realized on InₓGa₁₋ₓAs

**Channel**

- In₀.₅³Ga₀.₄₇As

- 0.3 nm AlOₓNᵧ interfacial layer

- 1nm Al₂O₃

- 2.5nm HfO₂

- Ni Gate

- 4nm
PLANAR MOS CV

- CET of 1.3 nm measured at 1 MHz
- Reduced frequency dispersion with FGA

MULTI-FIN SPLIT CV MEASUREMENT

- CET of 1.4 nm measured for multi-fin split CV structure
\[ Y_m = G_m + j\omega C_m \quad \sum_{\text{frequency}} Y_{\text{corrected}} - Y_m (D_{\text{IT}}, \tau, C_{\text{inv}}) = 0 \]

- Measured conductance and capacitance fitted iteratively using the equivalent circuit impedance
- Model self-consistently extracts distribution of \( D_{\text{IT}} \)

\[ D_{\text{IT}} : \text{EQUIVALENT CIRCUIT MODEL} \]

- Equivalent circuit method used to extract \( D_{\text{IT}} \)
EXTRACTED $D_{IT}$

- Mid-gap $D_{IT}$ reduced to $10^{12}$/cm$^2$/eV
- Fin sidewall $D_{IT}$ higher in conduction band

FINFET FABRICATION: XTEM

- Chemical component of RIE enhanced
- Fin taper changed to 70° from 85°
LONG CHANNEL FINFET PERFORMANCE

- SS improved from 180mV/dec to 100mV/dec
- $D_{it} = 8 \times 10^{12}$ estimated from calibrations and $2 \times 10^{12}$ from equivalent circuit model

OUTPUT CHARACTERISTICS

- Drive current increases with increasing In % and quantum confinement
**FIN MOBILITY**

Improved high-k interface with In$_{x}$Ga$_{1-x}$As allows accurate estimation of charge

<table>
<thead>
<tr>
<th>Channel Type</th>
<th>Mobility [cm$^2$/V*ns]</th>
<th>$n_s$ [x10$^{12}$ cm$^2$]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bulk</td>
<td>1500</td>
<td>$1x10^{12}$</td>
</tr>
<tr>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>2500</td>
<td></td>
</tr>
<tr>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As QW</td>
<td>3600</td>
<td></td>
</tr>
</tbody>
</table>

**SHORT CHANNEL DEVICES: SEM**

Short channel devices with gate recess opening down to 120nm realized
SHORT CHANNEL PERFORMANCE

- New gate stack implemented on short channel devices
- Significant improvement in SS from >200mV/dec to around 110mV/dec at \( L_g = 120\text{nm} \)

Symbol: experiment       Line: simulation

\( W_{\text{fin}} = 40\text{nm}; L_G = 120\text{nm}; 10\ \text{fins/\mu m} \)

- Drive current measured at 75\( \mu \text{A/fin} \) at \( V_G - V_T = 0.6\text{V} \) for \( \text{In}_{0.7}\text{Ga}_{0.3}\text{As QW FinFET} \)

OUTPUT CHARACTERISTICS

\( W_{\text{fin}} = 40\text{nm}; L_G = 120\text{nm}; 10\ \text{fins/\mu m} \)
Peak $g_m$ enhancement of 3.6x observed for QW In$_{0.7}$Ga$_{0.3}$As FinFET over bulk In$_{0.53}$Ga$_{0.47}$As FinFET

---

**SHORT CHANNEL SUMMARY**

<table>
<thead>
<tr>
<th>Channel Type</th>
<th>$I_{ON}$ @ $V_G - V_T = 0.6V$ $\mu A/\mu m$</th>
<th>SS $V_{DS} = 0.05V$ $mV$/dec</th>
<th>$g_m$ peak $mS/\mu m$</th>
<th>DIBL $mV/V$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bulk In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>250</td>
<td>105</td>
<td>0.490</td>
<td>221</td>
</tr>
<tr>
<td>QW In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>405</td>
<td>117</td>
<td>1.012</td>
<td>103</td>
</tr>
<tr>
<td>QW In$<em>{0.7}$Ga$</em>{0.3}$As</td>
<td>760</td>
<td>114</td>
<td>1.786</td>
<td>106</td>
</tr>
</tbody>
</table>
Q factor improves with higher In % and quantum confinement.
Q = 15 measured for In$_{0.7}$Ga$_{0.3}$As QW FinFET.
**G_m VS. SS BENCHMARKING**

- Q factor improves with higher In % and quantum confinement
- Q = 15 measured for In_{0.7}Ga_{0.3}As QW FinFET


**INJECTION VELOCITY**

- V_inj at virtual source extracted from simulations after calibration to experiments
- V_inj estimated at 1.4x10^7 cm/sec for In_{0.7}Ga_{0.3}As QW short channel FF at L_G = 120nm

Drive current projected to be 2.5x higher for In$_{0.7}$Ga$_{0.3}$As QW FinFET compared to silicon FF at $V_{DS} = 0.5V$ and fixed $I_{OFF} = 1nA/fin$

**Compound Semiconductor CMOS Challenge**

- Integrate III-V layers on large Silicon wafers
- Develop reliable high-K dielectric compatible with III-V
- Determine PFET (Ge) to go with NFET
- Insertion at 7nm node or beyond. Meet $L_G < 15$ nm and gate pitch less than 45nm with $W_{fin} < 5nm$

III-V ballistic FETs will have to simultaneously meet multiple requirements to be serious contenders as replacement for today’s state of art strained Si, Hi-K/MG, Tri-Gate transistors.
Low-Dimensional Systems for Device Applications

J. Appenzeller

Purdue University & Birck Nanotechnology Center
West Lafayette, IN 47907

Conference Sponsors:

ESSDERC 2015, September 14, 2015 - Tutorial

Nano is not just small …

Some general observations on the topic of Nano Electronics:

Normally people hunt for high mobility values …

… that is why carbon nanotubes and later graphene attracted so much attention!

Nano Electronics seems to still mainly focus on field-effect transistors!

Understanding the unique properties of transport in nano-systems is “less catchy”!
Nano is not just small …

<table>
<thead>
<tr>
<th>Material</th>
<th>Bulk Mobility</th>
<th>Bandgap</th>
<th>Effective Mass</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>cm²/Vs</td>
<td>eV</td>
<td>m*/m₀</td>
</tr>
<tr>
<td>GaN</td>
<td>2,000</td>
<td>3.47</td>
<td>0.2</td>
</tr>
<tr>
<td>Si</td>
<td>1,400</td>
<td>1.12</td>
<td>0.19</td>
</tr>
<tr>
<td>Ge</td>
<td>3,900</td>
<td>0.661</td>
<td>0.082</td>
</tr>
<tr>
<td>GaAs</td>
<td>8,500</td>
<td>1.424</td>
<td>0.067</td>
</tr>
<tr>
<td>InGaAs</td>
<td>12,000</td>
<td>0.74</td>
<td>0.041</td>
</tr>
<tr>
<td>InAs</td>
<td>40,000</td>
<td>0.354</td>
<td>0.023</td>
</tr>
<tr>
<td>InSb</td>
<td>70,000</td>
<td>0.17</td>
<td>0.014</td>
</tr>
<tr>
<td>graphene</td>
<td>100,000</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

(The numbers above are approximations that describe the trend - I do not claim them to be exact!)

Nano is not just small …

![Diagram](image)

effective mass ↓

band gap (off-state) ↓

mobility (on-state) ↑

carrier concentration (on-state) ↓
Nano is not just small …

Geometric screening and Schottky barriers

Geometric screening

\[
\frac{\partial^2 \phi(x,y)}{\partial x^2} + \frac{\partial^2 \phi(x,y)}{\partial y^2} = -\frac{\rho}{\epsilon_{body}}
\]

Note that:

\[
\phi_g = \phi_f + \frac{Q_S}{\epsilon_{ox}} \quad \text{and} \quad \epsilon_{body} \cdot E_S = Q_S
\]

assume:

\[
\phi(x,y) = C_0(x) + C_1(x) \cdot y + C_2(x) \cdot y^2
\]

\[
\frac{\partial \phi(x,y)}{\partial y} \bigg|_{y=0} = 0
\]

\[
\frac{\partial^2 \phi(x,y)}{\partial y^2} = C_1(x) + 2C_2(x) \cdot y = 2C_2(x) \cdot y
\]

\[
\frac{\partial^3 \phi(x,y)}{\partial y^3} = 2C_2(x)
\]
Geometric screening

\[ \frac{\partial^2 \phi(x,y)}{\partial x^2} + \frac{\partial^2 \phi(x,y)}{\partial y^2} = -\frac{\rho}{\varepsilon_{body}} \]

Note that:

\[ \varepsilon_{ox} \cdot \frac{\phi_g - \phi_f}{t_{ox}} = Q_S \quad \text{and} \quad \varepsilon_{body} \cdot \frac{\partial \phi(x,y)}{\partial y} \bigg|_{y = t_{body}} = Q_S \]

\[ \frac{\partial \phi(x,y)}{\partial y} \bigg|_{y = t_{body}} = \varepsilon_{ox} \cdot \frac{\phi_g - \phi_f}{\varepsilon_{body} \cdot t_{ox}} \]

\[ \frac{\partial^2 \phi(x,y)}{\partial y^2} = \frac{\varepsilon_{ox}}{\varepsilon_{body}} \cdot \frac{\phi_g - \phi_f}{t_{ox} \cdot t_{body}} \]

\[ \frac{\partial^2 \phi_f - \phi_f - \phi_g}{\partial x^2} \cdot \frac{\phi_f - \phi_g}{\lambda^2} = -\frac{\rho}{\varepsilon_{body}} \quad \text{with} \quad \lambda_{UTB} = \sqrt{t_{body} \cdot t_{ox} \cdot \frac{\varepsilon_{body}}{\varepsilon_{ox}}} \]

assume:

\[ \phi(x,y) = C_0(x) + C_1(x) \cdot y + C_2(x) \cdot y^2 \]

\[ \frac{\partial \phi(x,y)}{\partial y} \bigg|_{y=0} = C_1(x) + 2C_2(x) \cdot y = 2C_2(x) \cdot y \]

\[ \frac{\partial^2 \phi(x,y)}{\partial y^2} = 2C_2(x) \]
Another way to see the relevance of $\lambda$ for device scaling:

$$C_g > C_d$$

$$\varepsilon_{ox} \cdot \frac{W \cdot L_{ch}}{t_{ox}} > \varepsilon_{body} \cdot \frac{W \cdot t_{body}}{L_{ch}}$$

$$L_{ch} > \lambda$$

screening in bulk:

$$\lambda_{UTB} = \sqrt{t_{body} \cdot t_{ox} \cdot \frac{\varepsilon_{body}}{\varepsilon_{ox}}}$$

$$\lambda_{BULK} = \sqrt{W_{DM} \cdot t_{ox} \cdot \frac{\varepsilon_{body}}{\varepsilon_{ox}}}$$

Consider:

$t_{ox} = 5\text{nm}$, $\varepsilon_{body} = 12$, and $\varepsilon_{ox} = 4$:

$$\lambda_{UTB} = \sqrt{t_{body} \cdot t_{ox} \cdot \frac{\varepsilon_{body}}{\varepsilon_{ox}}}$$

$t_{body} = 1\text{nm}$

$$N_D = 10^{18}\text{cm}^{-3} \rightarrow W_{DM} \approx 25\text{nm}$$

$$\lambda_{UTB} \approx 4\text{nm}$$

UTB materials allow for aggressive channel length scaling!
Schottky barrier diodes

A simplified picture ...

Assuming a perfect contact from the source and no significant scattering contribution from the channel

Schottky barrier diodes

A simplified picture ...

Two back-to-back diodes result in “source limited” carrier injection for large $V_d$ and non-linear $I_d$-$V_d$ characteristics for small $V_d$
Schottky barrier diodes

A simplified picture …

Tunneling through SBs was ignored since $\lambda_{\text{BULK}}$ is too large

\[ \lambda_{\text{BULK}} = \sqrt{W_{DM} \cdot t_{ox} \cdot \frac{\varepsilon_{\text{body}}}{\varepsilon_{ox}}} \]

Schottky barrier diodes

A simplified picture … to illustrate the difference between BULK and UTB for device applications

Tunneling through SBs is the distinguishing aspect in nano-devices since $\lambda_{\text{UTB}}$ is frequently very small!

\[ \lambda_{\text{UTB}} = \sqrt{t_{\text{body}} \cdot t_{ox} \cdot \frac{\varepsilon_{\text{body}}}{\varepsilon_{ox}}} \]

\[ \lambda_{\text{BULK}} = \sqrt{W_{DM} \cdot t_{ox} \cdot \frac{\varepsilon_{\text{body}}}{\varepsilon_{ox}}} \]
A simplified picture … to illustrate the difference between BULK and UTB for device applications

Tunneling through $V_{gs}$-dependent SBs is the distinguishing aspect in nano-devices since $\lambda_{UTB}$ is frequently very small!

Strong tunneling currents create linear output characteristics! This is NOT an “Ohmic contact” since the transmission through the “tunneling” SB is gate voltage dependent!
Simulated output characteristics of a ballistic UTB SB-FET

Carbon Nanotube (CN) Field-Effect Transistor (FET)

Experimental output characteristics of an SB-MoS$_2$FET!

L = 200nm
t$_{OX}$ = 20nm
t$_{MoS2}$ = 8nm
T = 300K
Sc - contacts planar gated
Simulated subthreshold characteristics of an UTB SB-FET

Carbon Nanotube (CN) Field-Effect Transistor (FET)

Experimental subthreshold characteristics of an SB-CNFET

L = 300nm

t_{ox} = 10nm

t_{CN} = 1.8nm

T = 300K

Ti - contacts planar gated
Simulated subthreshold characteristics of an n-CN FET

Schottky barrier field-effect transistors

Understanding the impact of the SB on the inverse subthreshold slope:

Carbon Nanotube (CN) Field-Effect Transistor (FET)
Understanding the impact of the SB on the inverse subthreshold slope:

\[ S_{\lambda \to 0} = \frac{k_B T}{q} \ln(10) \]

\[ S \propto \lambda_{UB} \propto \sqrt{t_{ox} \cdot t_{body}} \]

\[ \lambda_{UB} = \sqrt{\frac{t_{body} \cdot t_{ox} \cdot \varepsilon_{body}}{\varepsilon_{ox}}} \]
Understanding the impact of the SB on the inverse subthreshold slope:

\[ S|_{\lambda \to 0} = \frac{k_BT}{q} \ln(10) \]

The voltage range over which the SB-regime occurs remains (almost) unaffected by the value of \( \lambda \)!

The inverse subthreshold slope also contains information about the SB height!

The SB height information is hidden in the voltage difference between \( V_{FB} \) and \( V_{th} \)!
The inverse subthreshold slope also contains information about the SB height!

Smaller $\Phi_{SB}$-values result in a smaller tunneling-current-impacted gate voltage window!

The inverse subthreshold slope does not change with $\Phi_{SB}$!

In reality the entire inverse subthreshold slope – including the thermal branch – is often also impacted by interface traps, making the identification of $V_{FB}$ difficult!
The inverse subthreshold slope also contains information about the SB height!

However, the actual $\Phi_{SB}$-value can be determined from the temperature dependence of the inverse subthreshold slope since the T-dependences of the thermal and the SB-regime are distinctly different!

**Procedure for $\Phi_{SB}$ extraction:**

+ Measure $I_d$-$V_{gs}$ as function of temperature
Procedure for $\Phi_{SB}$ extraction:
+ Measure $I_d-V_{gs}$ as function of temperature
+ Create gate voltage dependent Arrhenius plots

assuming thermal emission theory
Schottky barrier field-effect transistors

Procedure for $\Phi_{SB}$ extraction:
+ Measure $I_d-V_{gs}$ as function of temperature
+ Create gate voltage dependent Arrhenius plots
+ Extract “apparent” barrier versus gate voltage assuming thermal emission theory
+ Determine the “real” SB-height at $V_{FB}$


Nano is not just small …

An example:
SB-FETs from MoS$_2$

S. Das et al., Nano Letters 13, 100 (2013).
Various contact types to MoS$_2$

The metal work function does not entirely determine the Fermi-level line-up to MoS$_2$
SB-FETs – MoS₂

Fermi-level pinning in MoS₂

\[ \frac{d\Phi_{SB}}{d\Phi_M} \approx 0.1 \]

Si with silicide: 150 Ω-μm

\[ R_{C-Sc} \approx 500 \text{ Ω-μm} \quad \text{for } t_{ox}=5\text{nm} \]

Nano is not just small …

Data extraction using an analytical SB-model
But the Schottky barrier height cannot always be extracted in this way:

Schottky barrier field-effect transistors

SB-FETs – WSe$_2$

But the Schottky barrier height cannot always be extracted in this way:
SB-FETs – WSe₂

But the Schottky barrier height cannot always be extracted in this way …

... then more complete simulations are required to extract band gap and Schottky barrier information ...

An analytical SB model

Example “electron current”:

\[ I_d = \frac{2q}{h} \int_{E_c}^{\infty} T(E) \cdot M_c(E) \cdot [f(E) - f(E - qV_{ds})] \, dE \]

\[ M_c(E) = \frac{g_c}{\pi h} \sqrt{2m^*_c (E - E_c(V_{gs}))} \]

\[ T_{WKB}(E) = \exp \left( - \int_{x_m}^{x_0} \kappa(E) \, dx \right) \]

\[ \kappa(E) = \frac{1}{h} \sqrt{2m^*_c (E_c(x) - E)} \]
An analytical SB model

The impact of the Schottky barrier height on the on/off-current ratio:

For the same $E_g$, an apparently smaller on/off-current ratio is obtained for a Fermi level alignment closer to midgap!

An analytical SB model

The impact of the geometric screening length on the transfer characteristics of SB-FETs:

The smaller $\lambda$, the more symmetric ambipolar device characteristics occur independent of the SB-height!
Schottky barrier field-effect transistors

Related Publications (presenter’s choice):


Nano is not just small …

The tunneling field-effect transistor (TFET)
The quantum capacitance

In addition to the geometric screening length $\lambda$, also the density of states in low-dimensional nanostructures can be substantially different from conventional materials!

\[ C_{\text{tot}} = e \frac{\partial Q_{\text{tot}}}{\partial \Phi_g} = \frac{C_{\text{ox}} C_q}{C_{\text{ox}} + C_q} \quad C_q = e \frac{\partial Q_{\text{tot}}}{\partial \Phi_f} \]

\[ \delta \Phi_f^0 = \frac{C_{\text{ox}}}{C_{\text{ox}} + C_q} \cdot \delta \Phi_g \]

\[ C_{\text{q}1D} \approx e^2 L T_{\text{SB}} \left( E_f^s - \Phi_f^0 \right) D_{\text{1D}} \left( E_f^s - \Phi_f^0 \right) \]

+ Since $C_q$ can be very small in 1D structures, FETs become band rather than charge controlled devices!
\[(\text{even in the on-state})\]
+ SB devices are frequently found to operate in the quantum capacitance limit (QCL)!  

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The tunneling field-effect transistor

Combining the advantages of low-dimensional systems:

+ Ultra-thin body
  \[ \lambda_{UTB} \rightarrow \text{thin tunneling barrier} \]
+ Operation in the quantum capacitance limit
  \[ \rightarrow \text{one-to-one band movement} \]

Develop a device concept that makes use of the intrinsic properties of low-dimensional systems!

Simulated gate voltage response of a T-CNFET

The device on-state involves band-to-band tunneling!
The tunneling field-effect transistor

Simulated gate voltage response of a T-CNFT

The device on-state involves band-to-band tunneling!

Nano is not just small ...

Thank you!