

Structural, Morphological and Electrical Properties of Pentacene Based Thin Film Transistors

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Introduction

Similar to other organic materials pentacene has a strong tendency to form weakly bound van-der-Waals molecular single crystals and highly ordered polycrystalline thin films. During the growth process the molecules arrange in a herringbone structure within each elementary cell. In the thermodynamic limit the growth morphology is determined by the balance of the interfacial free energies involved. For temperatures far from thermodynamic equilibrium, the thin film morphology will be governed by kinetic effects. If the interlayer mass transport is fast enough to allow atoms to leave the tops of growing 2D islands as soon as they arrive, the growing layer will be completed before second layer nucleation sets in and smooth layer-by-layer growth results. If, however, the interlayer mass transport is hindered by a sufficiently large diffusion barrier at the island edge, growth in the next layer starts before the previous one is filled and 3D structures develop (multilayer or 3D growth). As the nucleation density of the first crystalline molecular layer is determined by the ratio of the growth rate to the diffusion constant of pentacene on the substrate, high evaporation rates and poorly controlled surfaces with a lot of reactive bonds result in enhanced layer-by-layer growth and smooth densely packed films with small grains and a high grain-boundary density.

Thin Film Formation and Substrate Material

In Fig. 1 the early stages of pentacene thin film formation are demonstrated by atomic force microscopy. The 1.4 nm thick film is composed of densely packed well-separated 2D islands each representing a single crystal. The step height variation over the film corresponds to the c-axis length of pentacene of approximately 1.5 nm. In the 3.5 nm thick film the islands of the first monolayer have been coalesced and a second monolayer has started to nucleate on top of some islands. This is due to the fact that nucleation of the second layer takes place not before the islands in the first layer have exceeded a critical size. The 7 nm thick film shows 3D branched terraced crystals with step heights of 1.5 nm that can be associated with the large dendritic crystallites that are observed with optical microscopy for films grown under ultra-high vacuum conditions near the thermodynamic equilibrium (background image). 3D island growth is observed for many substrates including SiO_2 and a lot of organic materials such as polymethylmetacrylate (PMMA), polyvinylphenol-copolymer (PVP) and polyvinylcinematester (PVCi) (Fig. 2). It is interesting to note that the average grain size increases continuously in going from SiO_2 to PVCi due to a decreasing nucleation density in the early stages of the 3D island growth process. This could be an effect of the lower density of reactive sites on the organic substrates yielding higher diffusion constants.

Substrate Temperature and Pentacene Polymorphs

An increase of the substrate temperature during the condensation process usually leads to an increase in the average and the maximum grain size (Fig. 3). This is due to the fact that for higher temperatures the mobility of molecules arriving at the surface is increased resulting in a better alignment of the molecules, a faster edge diffusion and a lower nucleation density. However, the correlation between substrate temperature and grain size is not straightforward because other processes are also influenced by temperature. Thermal desorption plays a role together with temperature-induced phase transformation processes and changes in the volume fraction of the different pentacene phases. These effects are responsible for the differences in grain size and shape observed for the film deposited at 65°C – 70°C compared to the one at 25°C . At higher temperatures where edge diffusion is increased the crystallites are rather square and obviously larger than for the deposition at 25°C , where the grains show a ramified shape. The decrease in grain size for the 75°C film, however, could be due either to the increasing volume fraction of the bulk phase or to thermal desorption. From growth experiments on PVP, where pentacene forms single phase thin films even at elevated substrate temperatures it can be concluded that the maximum grain size is achieved for temperatures between 62°C and 68°C (Fig. 4). The increase of the grain density for higher growth temperatures seems to be due to an increase in the ratio of desorbing to diffusing molecules. It should be mentioned that we observed another critical parameter concerning the pentacene phase formation, which is the film thickness. With increasing film thickness the fraction of the thermodynamically more stable bulk phase increases with respect to the thin film phase.

Deposition Rate

In the atomic force images of Fig. 5 the influence of a reduction of the deposition rate is illustrated. It is clearly visible that decreasing the deposition rate not only increases the grain size but also changes the surface morphology of the films from an assembly of squared to one of ramified grains. For a given substrate material and a given temperature it is preliminary the deposition rate at the initial stages of the nucleation process that determines the nucleation density. For a control of the growth process, it is inevitable to precisely adjust the deposition rate. The grain density and the maximum grain size show a clear power law dependence on the initial deposition rate with exponents that are closely related to each other by a factor of two and, as nucleation theory tells us, are characteristic for the "extreme incomplete condensation" regime for a critical molecular cluster size of 2 (Fig. 6).

Electrical Characterization

All investigated thin film transistors are constructed in the common-gate configuration with source and drain on top. The electrodes are made by thermal evaporation of gold through a shadow mask. From the input characteristics (Fig. 7) the mobility in the saturation regime can be extracted by assuming the phenomenological quadratic dependence of the drain current on the gate voltage that is typical for accumulation-type field effect transistors. A respective analysis of the data reveals a carrier mobility that is strongly increasing with increasing gate voltage due to the filling of traps up to a value called trap-filled limited mobility μ_0 (Fig. 8). This maximum mobility μ_0 , however, is linearly depending on the drain voltage (Fig. 10). A field dependent trap-filled limited mobility can be described within a field-activated transport model. In Fig. 9 the influence of the gold deposition rate is illustrated. Fast deposition seems to form contacts with smaller resistances than slow one, which is reflected by the higher On/Off ratio, the smaller subthreshold slope, and the smaller threshold voltage, as well as the higher mobility (Fig. 10). Comparing the μ_0 with the size of the crystallites leads to a surprising correlation (Fig. 11). If the pentacene layer of a transistor (with SiO_2 as dielectric) consists of grains with average size below $1\ \mu\text{m}$ then the mobility is very low ($\sim 10^{-2}\ \text{cm}^2/\text{Vs}$). Around $1\ \mu\text{m}$ one observes a steep increase in the mobility, which levels for larger crystallites. Such a threshold behavior can be expected if the carrier mean free path is about $1\ \mu\text{m}$ resulting in increased surface scattering and grain boundary effects for fine granular layers. Above this threshold an increase in grain size does not drastically increase the mobility. A similar correlation is observed for PVP. Here the mobility can be increased by a factor of at least 2 by increasing the substrate temperature, which yields substantially larger grains, as can also be deduced from Fig. 4.

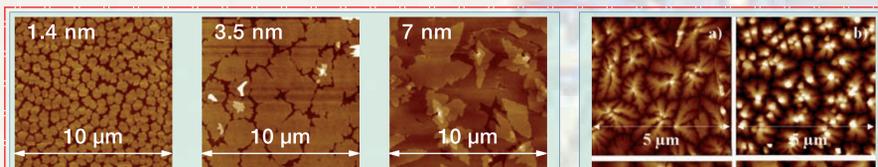


Figure 1: Atomic force microscopy (AFM) images of the first few monolayers on a SiO_2 substrate. The deposition rate R was less than $1\ \text{nm}/\text{min}$ and the substrate temperature was 65°C .

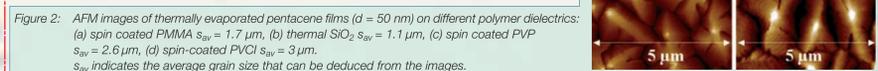


Figure 2: AFM images of thermally evaporated pentacene films ($d = 50\ \text{nm}$) on different polymer dielectrics: (a) spin coated PMMA $S_{av} = 1.7\ \mu\text{m}$, (b) thermal SiO_2 $S_{av} = 1.1\ \mu\text{m}$, (c) spin coated PVP $S_{av} = 2.6\ \mu\text{m}$, (d) spin-coated PVCi $S_{av} = 3\ \mu\text{m}$. S_{av} indicates the average grain size that can be deduced from the images.

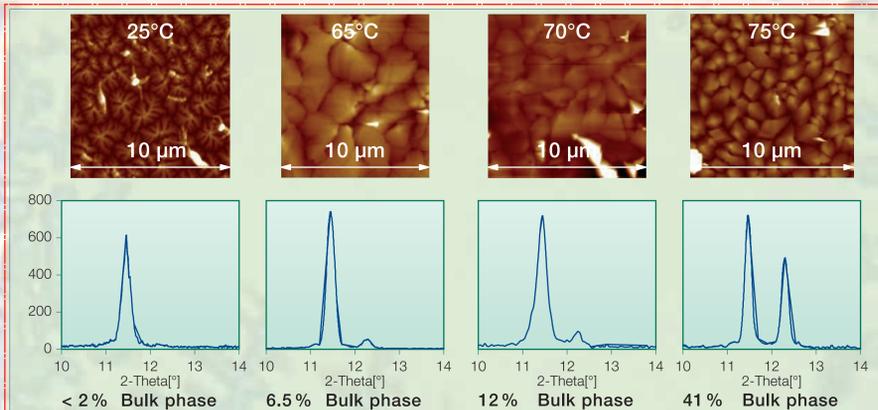


Figure 3: AFM images of pentacene films ($d = 50\ \text{nm}$) evaporated on thermal SiO_2 at different temperatures and for $R = 1\ \text{nm}/\text{min}$. The inserts show the (002)-reflexes of the respective x-ray diffraction pattern.

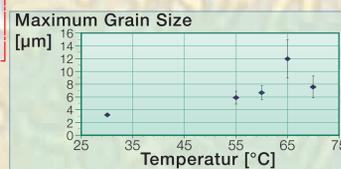


Figure 4: Grain size distribution of pentacene as a function of the substrate temperature. The biggest grains grow at 65°C . The substrate material was PVP.

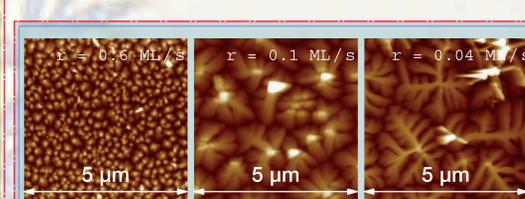


Figure 5: Comparison of AFM images of pentacene thin films on silicon dioxide deposited at different initial rates and room temperature.

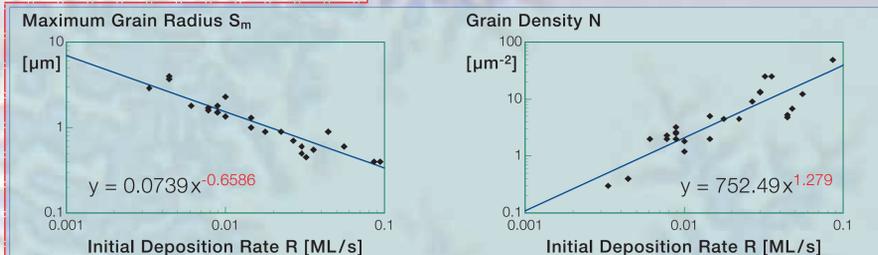


Figure 6: Correlation between the initial deposition rate and (a) the grain density N and (b) the maximum grain size S_m for $50\ \text{nm}$ thick pentacene thin films grown at room temperature on thermal SiO_2 . Note that the power coefficient for S_m is nearly half as large as the one for N .

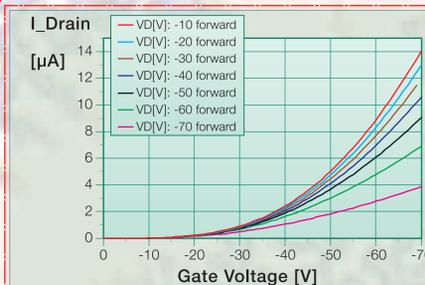


Figure 7: Input characteristics of an organic field-effect transistor with PVP as dielectric.

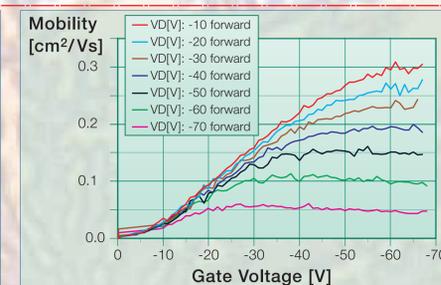


Figure 8: Gate voltage dependence of the charge carrier mobility of an organic field-effect transistor with PVP as dielectric. The influence of the drain voltage is also illustrated.

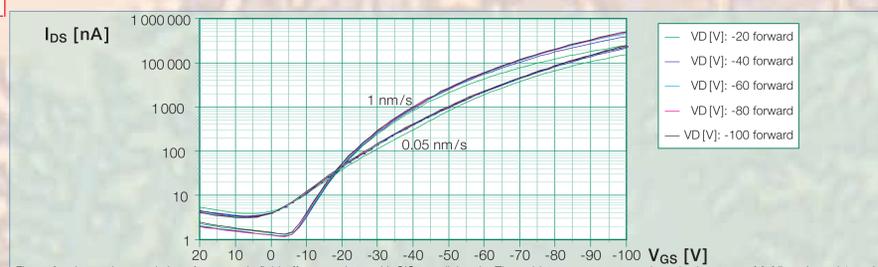


Figure 9: Input characteristics of an organic field-effect transistor with SiO_2 as dielectric. The gold top contacts were deposited at rates of $0.05\ \text{nm}/\text{s}$ and $1\ \text{nm}/\text{s}$.

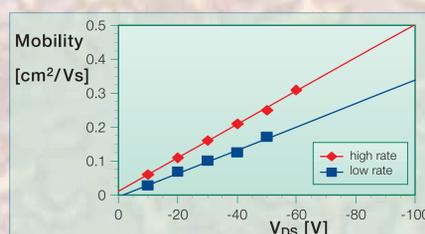


Figure 10: Drain voltage dependence of the trap filled limited mobility of the devices from Fig. 9.

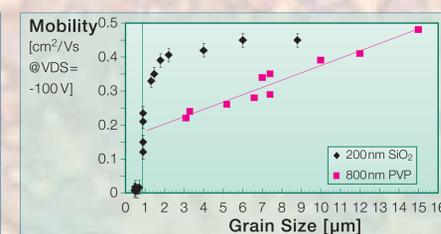


Figure 11: Grain size dependence of the mobility for thin film transistors with SiO_2 and PVP as dielectric.

