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Structuring of oFETs with hot-embossing

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Structuring of organic field-effect-transistors with hot-embossing

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In this work we present organic thin film transistors using the polycyclic aromatic molecule pentacene as semiconductor in common-gate geometry. We compare various structuring techniques for source and drain such as shadow masks, inkjet printing and hot embossing. We used SiO_2 as the dielectric layer to have a good starting point for the optimization of the structuring processes; after the best structuring parameters were found, we switched to the organic gate dielectric materials PVP, PMMA, etc. For shadow mask structuring silicon or gold was used as gate material, pentacene was evaporated on the gate dielectric with the optimized deposition parameters, and gold source–drain contacts were applied to the semiconductor layer by e-beam evaporation. As a second example we show an all-organic inkjet printed oFET, the source–drain structures were made of polyaniline. For the hot embossing process the source–drain material (gold or PEDOT) was deposited on a flexible substrate (PET) and structured using the nanoimprint resist PMMA and a subsequent reactive ion etch step. For this purpose a 1µm thick PMMA layer was spincoated on the (organic) metal and imprinted for 5 minutes at a temperature of 210°C and a pressure of 175 bar, the chamber was evacuated to 0.2 mbar. The used imprinting tool was an EVG501. Subsequently the resist was stripped with acetone. In the final step this source–drain structure on the flexible substrate was applied to a gate–dielectric–semiconductor–complex (consisting of a highly doped silicon gate covered by the (organic) dielectric layer and the organic semiconductor pentacene) by soft contact lamination[1].

The electrical output and transfer characteristics of the fabricated transistors were measured with a parameter-analyser to evaluate the transistor performance depending on the structuring conditions. As a first step for the realization of printed contacts we used inkjet-printing and achieved mobilities of approx. 0.15 cm^2/Vs for the all-organic-FET. With gold-contacts and PVP as the gate-dielectric, mobilities of >1 cm^2/Vs in the oFET and on-off-ratios of >10^5 have been achieved reproducibly. The optimization of the deposition parameters used in the thermal evaporation process influencing the grain morphology and the knowledge about the relation between grain-size and hole-transport-properties of the pentacene layer give us the possibility to fabricate organic field-effect-transistors with well-defined electronic properties and field effect mobilities around µ=1cm^2/Vs.

Shadow Mask Structuring

Gate-dielectric: SiO_2

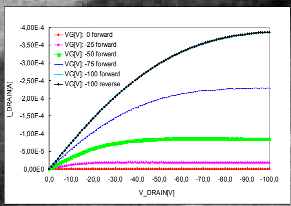
Fig.1: Output characteristics of SiO2 oFET

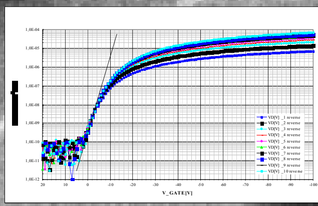
Fig.2: Transfer characteristics of SiO2 oFET

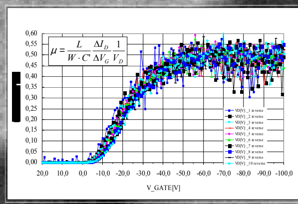
Fig.3: Mobility vs.gate voltage of SiO2 oFET

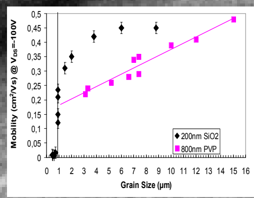

Fig.4: Mobility vs. Pentacene grain size for SiO2 resp. PVP oFETs

Gate-dielectric: PVP

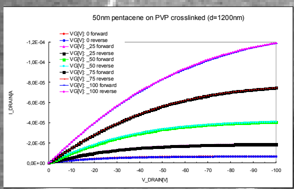

Fig.5: Output characteristics of PVP oFET

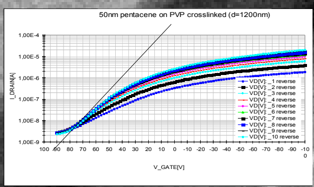

Fig.6: Transfer characteristics of PVP oFET

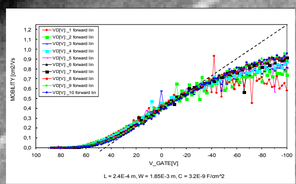
Fig.7: Mobility vs.gate voltage of PVP oFET

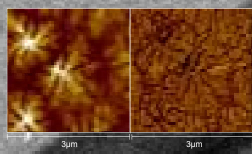

Fig.8: AFM image (a: height signal b: phase signal) of a pentacene layer on PVP

All Organic Transistor – Inkjet Printing

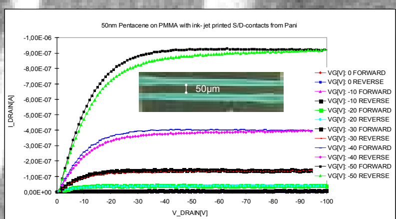

Fig.9: Output characteristics of all-organic oFET

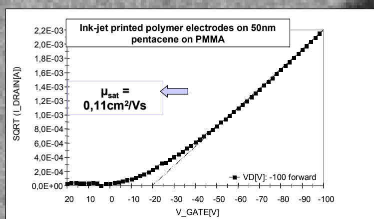

Fig.10: Transfer characteristics of all-organic oFET

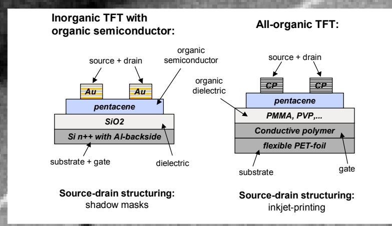

Fig.11: schematic design of oFETs

Hot Embossing – Soft Contact Lamination

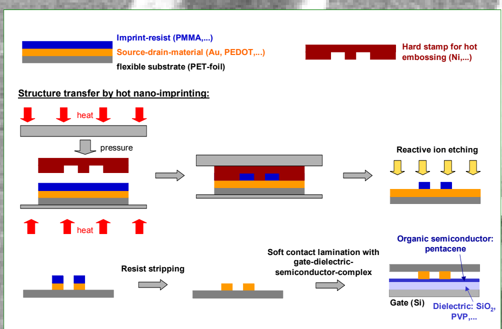

Fig.12: Structuring process for oFETs by hot embossing and soft contact lamination

Various patterns structured by hot embossing

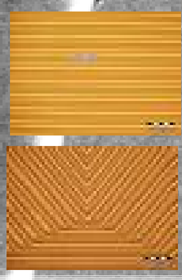
Fig.14: gold structures on PET, directly


Fig.15: PEDOT structures on PET, directly

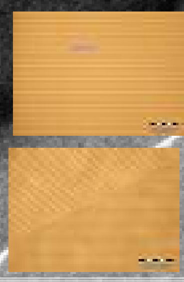
Fig.16: gold structures on PET, using PMMA as imprint resist

a TRADITION of INNOVATION

[1] Zaumseil et al., *Journal of Applied Physics 2003*, Vol. 93, **10**, *6117-6124*

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